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Abstract
In recent year, the Surrounding/Cylindrical-Gate SOI MOSFET's has attracted a lot of attention and become a potential candidate for the VLSI due to the following advantages: (1) high packing density and high performance (2) reduced short-channel effects and hot carrier effects (3) ideal subthreshold swing and lower channel leakage current By wrapping the gate completely around the channel, the gate gains increased control of the potential in the channel. As semiconductor devices are scaled into to the deep submicron-meter regime, surrounding/cylindrical-gate SOI MOSFET's have shown promise in both the short-channel effect and in achieving a nearly ideal subthreshold slope. The main short-channel effects consist of (1) Drain-Induced Barrier Lowering effect (DIBL), (2) Threshold voltage roll-off (3) Subthreshold slope degradation To control the Surrounding/Cylindrical-Gate SOI MOSFET's very well, when they are applied to the VLSI, there is a need to develop a accurate model for the subthreshold behavior. Therefore, the main goal of the thesis will focus on the analysis of the subthreshold behavior and present a reliable analytical model of the subthreshold characteristics. The thesis will comprise four chapters:
Chapter 1, The basic idea of the fully-depleted surrounding/cylindrical-gate SOI MOSFET's including the structure of the 2D and 3D and its advantages in recent advanced devices.
Chapter 2, A brief introduction in MEDICI simulation program.
Chapter3, To develop a he physically reliable model for the fully-depleted surrounding/cylindrical-gate SOI MOSFET's. The model comprises Drain-Induced Barrier Lowering effect (DIBL), threshold voltage roll-off and subthreshold slope.
Chapter 4, Conclusions and future works.
Advisory Committee T.K. Chiang - advisor

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